

AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please cancel claim 8 without prejudice.

1. (CURRENTLY AMENDED) An apparatus comprising:

a plurality of configuration pins configured to receive  
a plurality of configuration signals generated external to said  
apparatus;

5 an input pin for data; and

a circuit comprising:

a first logic gate configured to generate a first  
identification signal from said configuration signals;

a first multiplexer directly connected to said first  
10 logic gate to multiplex said first identification signal to a first  
multiplexer output; and

a shift register comprising a plurality of memory  
elements, wherein (i) said shift register is couplable to said  
input pin and (ii) a first of said memory elements has a first  
15 input directly connected to said first multiplexer output such that  
said first identification signal forms a first portion of a device  
identification for said apparatus.

2. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said configuration signals are user variable.

3. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said circuit comprises a JTAG compliant controller.

4. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein each value of said device identification identifies a unique configuration of said circuit.

5. (PREVIOUSLY PRESENTED) The apparatus according to claim 4, wherein said device identification determines a storage capacity of said circuit.

6. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said circuit further comprises:

a second logic gate configured to generate a second identification signal from said configuration signals and;

5 a second multiplexer directly connected to said second logic gate to multiplex said second identification signal to a second multiplexer output, wherein a second of said memory elements has a second input directly connected to said second multiplexer

output such that said second identification signal forms a second  
10 portion of said device identification.

7. (PREVIOUSLY PRESENTED) The apparatus according to claim 6, wherein said second multiplexer is directly connected to a first memory output of said first memory element.

8. (CANCELED)

9. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said circuit further comprises a FIFO memory.

10. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said configuration signals comprise mark options.

11. (CANCELED)

12. (ORIGINAL) The apparatus according to claim 1, wherein said circuit comprises a JTAG device compliant with the IEEE standard 1149.1.

13. (CURRENTLY AMENDED) An apparatus comprising:  
means for receiving a plurality of configuration signals generated external to said apparatus;

an input pin for data;

5 means for generating a first identification signal from said configuration signals;

means for multiplexing said first identification signal from said means for generating to a first output; and

10 means for storing a plurality of bits (i) couplable to said input pin, wherein (ii) a first of said means for storing has a first input directly connected to said first output such that said first identification signal forms a portion of a device identification for said apparatus.

14. (CURRENTLY AMENDED) A method for selecting a device identification for an apparatus, comprising the steps of:

(A) receiving a plurality of configuration signals generated external to said apparatus at a plurality of  
5 configuration pins;

(B) generating a first identification signal by performing a logic operation on said configuration signals;

(C) multiplexing said first identification signal to a first memory element of a plurality of memory elements in a shift  
10 register couplable to an input pin for data; and

(D) storing said first identification signal in said first memory element such that said first identification signal forms a first portion of said device identification.

15. (PREVIOUSLY PRESENTED) The method according to claim 14, wherein said configuration signals are user variable.

16. (PREVIOUSLY PRESENTED) The method according to claim 14, wherein each value of said device identification identifies a unique configuration of said apparatus.

17. (PREVIOUSLY PRESENTED) The method according to claim 14, wherein said device identification determines a storage capacity of said apparatus.

18. (PREVIOUSLY PRESENTED) The method according to claim 14, wherein said configuration signals comprise mark options.

19. (CANCELED)

20. (PREVIOUSLY PRESENTED) The method according to claim 14, wherein said apparatus is a JTAG device compliant with the IEEE standard 1149.1.

21. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, further comprising an output multiplexer configured to

multiplex said device identification from said shift register to an output pin.

22. (PREVIOUSLY PRESENTED) The method according to claim 14, further comprising the step of:

multiplexing said device identification from said shift register to an output pin.